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SPECIFICATION

INVENTION: **PROGRAMMABLE BANDWIDTH AND FREQUENCY SLEWING FOR PHASE-LOCK LOOP**

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CROSS-REFERENCE

[0001] This application claims the benefit of U.S. Provisional Application No. 60/536,398, filed January 14, 2004; is related to U.S. Application No. 10/264,360 entitled PHASE-LOCK LOOP HAVING PROGRAMMABLE BANDWIDTH and U.S. Application No. 10/264,359 entitled PWM CONTROLLER WITH INTEGRATED PLL, both of which were filed on October 4, 2002; and all of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

[0002] A graphics board is a printed-circuit board that typically includes at least one graphics processor and other electronic components that process and display graphics or other video data in a computer system. Figure 1 is a block diagram of a graphics board 100 that includes a graphics processor 105, as discussed in the aforementioned U.S. applications. Typically, one of the electronic components connected to the graphics processor 105 is a double-data-rate random-access memory (DDS RAM) chip 106. Both the graphics processor 105 and the DDR RAM 106 typically have high power requirements, as compared to other electronic components. For example, the graphics processor 105 typically requires 5-15 amps (A) of power at 1.6 volts (V), and the DDR RAM 106 typically 5-10 A and 10-20 A at 1.25 V and 2.5 V, respectively. Because the processor 105 and DDR RAM 106 have such high power requirements, pulse-width-modulated (PWM) switching power supplies 110a, 110b, and 110c are typically provided for the graphics processor 105 and the DDR RAM 106. A common power supply 108 feed the PWM switching power supplies 110a, 110b and 110c. Typically, the PWM power supplies 110a, 110b and 110c each includes a separate PWM-controller chip 112a, 112b and 112c, although these controllers can be integrated into the graphics processor 105 and DDR RAM 106 chips, respectively.

[0003] Ideally, the operating frequencies of the PWM power supplies 110a, 110b and 110c are the same. If, however, these frequencies are different, undesirable "beat" frequencies can result. A beat frequency is equal to the difference between the two frequencies. Unfortunately, the beat frequency can cause undesirable artifacts to appear in a video display.

[0004] A technique for reducing or eliminating the beat frequency is for two of the PWM controllers 112b and 112c (slaves) of the graphics board 105 to lock onto the PWM signal of the other PWM controller 112a (master) using a phase-lock loop

(PLL). The slave PLLs can each generate one or more slave-PWM output signals that are phase locked to the master-PWM signal and that have the same frequency as the master-PWM signal.

[0005] As illustrated in Figure 2, the master-PWM controller 112a provides output signals UG and LG to driver 120a, which provides a signal to integrator 122a. The output of the integrator 122a is V1. The master-PWM controller 112a also has signal LG connected as the input to a slave-PWM 112b. The output signals UG and LG of the slave-PWM 112b are provided to driver 120b, which provides a signal to integrator 122b. The output signal is V2. The slave-PWMs have a tendency to overcorrect if there are disturbances on the input signal. In other systems wherein the input signals to the PWM controllers are a crystal oscillator, there are no missed pulses. However, in PWM master/slave applications, there are missed pulses if the load current is stepped. If there are few missing pulses, it is possible that either the up or down pulses in the pulse width in the PLL will be very wide and drive the voltage control oscillator (VCO) to follow.

[0006] An example of this type of PLL is illustrated in Figure 3 and disclosed in detail in the aforementioned U.S. applications. The input or reference signal IN2 at 202 is provided to a phase frequency detector (PFD) 200. The input signal 202 is compared against a feedback signal 204 coming from VCO 206. Depending upon the frequency difference, an up signal UP 208 or a down signal DN 210 is provided through a switching, gate or logic circuit 212 as UPG and DNG to a charge pump 220. The output of the charge pump 220 is provided through a filter 226 to the VCO 206. The output of VCO 206 is the output signal IN1 at 234, as well as feedback signal 204. A ÷ N counter 218 is responsive to the cycles of the PFD 220 to transmit the up/down signals on 208 and 210 through the gate circuit 212 to operate the charge pump 220. In the above-mentioned applications, the circuit 212 is shown as gated inverters, as well as multiplexes. In Figure 3, they are illustrated by AND gates 214, 216. It should also be noted that the filter 226 has capacitor 228 in parallel with the series connection resistor 232 and capacitor 230. ÷ N counter 218 is a decrementing counter and maintains a transmission signal having a width of a cycle of the PFD 220. It is the width of this signal through the circuit 212 which causes the overcorrection for the instability in the input signal at 202.

SUMMARY OF THE INVENTION

[0007] One embodiment is a PLL which includes an oscillator having an oscillator signal whose frequency is related to a received error correction signal and PFD receiving and comparing the oscillator signal and a reference signal from a master circuit and generating the error correction signal based on the phase difference of the oscillator signal and the reference signal. A first window circuit counts the number of comparing cycles of the detector and provides a first window signal for the transmission of the error correction signals from the detector to the oscillator at a frequency of a predetermined number of counted comparing cycles. A second window circuit which, in response to at least the oscillator signal, narrows the first window signal to limit the duration of the correction signal for irregular reference signals.

[0008] The second window circuit may include a delayed path delayed with respect to a generally non-delayed path for the respective signal and a first logic circuit responsive to the delayed and non-delayed signals to produce the second window signal which narrows the first window signal. A second logic circuit responsive to the first and second window signals to transmit the error correction signals from the detector to the oscillator may also be provided. The PLL may include a rate selector circuit, which monitors and adjusts the predetermined number of counts as a function of the error correction signal.

[0009] The PLL may be provided in a slave-PWM controller of a pulse width modulated system wherein the reference signal is from the master-PWM controller, and the oscillator proves a PWM signal. Also, the pulse width modulation system may be part of a power supply circuit having master and slave power supplies. The power supply may be part of a video processor, which may be part of a computer system. The PLL may be provided in a transmitter/receiver.

[00010] These and other aspects of the present disclosure will become apparent from the following detailed description of the disclosure, when considered in conjunction with accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[00011] Figure 1 is a block diagram of a graphic board that utilizes an embodiment of a PWM controller according to an embodiment of the present disclosure.

[00012] Figure 2 is a schematic of a master/slave PWM controller.

[00013] Figure 3 is a schematic of a type of PLL to which the present disclosure is directed.

[00014] Figure 4 is a schematic of a PLL incorporating the principles of the present disclosure.

[00015] Figure 5 shows graphs of signals at various points in the PLL of Figure 4 for a locked condition of the loop.

[00016] Figure 6 is another embodiment of PLL incorporating the principles of the present disclosure to accommodate fluctuations in the input signal.

[00017] Figure 7 is a block diagram of an even further embodiment of the PLL, according to the present disclosure, with a variable rate of the transmission of the correction signal.

[00018] Figure 8 is an even further embodiment of the PLL, according to the present disclosure, showing a further variable rate of transmission of the correction signal.

[00019] Figure 9 is a schematic of a PLL incorporating the embodiments of Figure 4 and Figure 7 or Figure 4 and Figure 8.

[00020] Figure 10 is a diagram of a Wireless-Area-Network (WAN) transmitter/receiver that can incorporate the PLL of the present disclosure.

[00021] Figure 11 is a block diagram of a computer that incorporates the graphic board of Figure 1 with one of the PLLs of the present disclosure.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[00022] The PLLs of the present disclosure may be used in the graphic card 100 of Figure 1, the slave PWM controller 112b of Figure 2, the WAN transmitter/ receiver of Figure 10 or the computer of Figure 11. They may also be used in other devices requiring a PLL. Figures 4 and 6 show embodiments of a PLL wherein the width of the correction pulse is limited. This prevents the irregularity of the reference or input signal from causing a locked loop to start corrections or an unlocked loop to overcorrect. The embodiments of Figures 7 and 8 are PLLs with a variable rate of transmission of the correction signal. Figure 9 is a combination of the embodiments having a limited duration of the correction signal and a variable rate of transmission.

[00023] Those elements of the PLL which are common to that shown of Figure 3 will have the same reference numbers and function the same way as those elements in Figure 3. The operation of the PLL including the phase frequency detector

(PFD) 200, the counter 218, the logic transmission circuit 212, the charge pump 220, the filter 226 and the VCO 206 are well known and will not be described in detail. Reference will be made to the aforementioned applications, as well as other prior art devices.

[00024] As previously described with respect to Figure 3, the frequency of the correction pulses UPG and DNG are defined by the period in which the output of the counter 218 activates the gates 214 and 216 and transmits the signal to the charge pump 220. This frequency is a function of the frequency of the input signal 202 and the feedback signal 234 at input 204. The present system offers a second window circuit 300, which is applied to the gating or transmission circuit 212 to limit the width of the first window en_pfd WIN1 from the counter 218 to the width of the second window WIN2 produced by the second window circuit 300.

[00025] The first embodiment of the second window circuit 300 is illustrated in Figure 4. The window circuit 300 includes a first second window circuit 310. The oscillator output signal IN1 at output 234 is provided through feedback as a first input to NOR gate 312. The other input to NOR gate 312 is the signal IN1 through a time delay circuit 314 and inverter 316. The output of the NOR gate 312 is a pulse having a width of the time delay 314. The time delayed feedback signal is also provided to the PFD 220 as signal $\overline{IN1}$ on 318. A second second window circuit 320 provides a signal in response to the reference or input signal IN2 at input 202. Input signal 202 is provided to a NOR gate 322, whose other input is the input signal IN2 through time delay circuit 324 and inverter 326. The input signal IN2 at 202 through time delay 324 is also provided as the reference input signal $\overline{IN2}$ on 328 to the PFD 220.

[00026] The output of NOR gates 312, 322 are provided to OR gate 330. The output of OR gate 330 is a window 2 signal WIN2, which is provided to each of the AND gates 214 and 216 to be combined with the up or down correct signals UP, DN on 208 or 210 and the output of the counter circuit 218, which is enable-PFD or window 1 (WIN1). Thus, for example, if counter 218 is set for 16, on every 16^{th} pulse, the window 1 signal will be high for a period between the count signals cnt. The AND gates 214, 216 will not transmit the up/down signals, even though counter 218 is high, until it receives the second window signal window 2 from OR gate 330. The length of transmission through the gates 214, 216 is a

function of the width of the second window signal window 2, which is equal to the time delay Δt of the time delay circuits 314 or 324.

[00027] Although the second window signal window 2 is responsive to either the feedback or oscillator signal IN1 or the input signal IN2 and both are shown in Figure 4, not both signals are needed. The feedback or oscillator signal IN1 alone may be used. The use of the feedback signal IN1 allows the gating of the gates 214, 216 for erratic input signals IN2 at input 202. As previously discussed, the count signal out of the PFD 220 to counter 218 is once per comparison cycle. Also, the window 2 pulse is once per cycle.

[00028] Since the pulse width of window 2 is defined merely by a time delay 314 or 324, it does not vary based on the change of frequency of the input signal or the frequency of the VCO 206. It should also be noted that, with the specific structure shown, the PLL works on the falling edge of the signals.

[00029] Figure 5 shows graphs of the various signals in the PLL of Figure 4. The first three graphs show the relationship of the oscillator signal IN1, the window 2 signal of the window 2 loop 310 and the oscillator input signal $\overline{IN1}$ into the PFD 220. The next three graphs show the relationship between the reference or input signal IN2, the delayed input signal $\overline{IN2}$ to the PFD 220 and the window 2 signal from the window 2 circuit 320. The next two graphs show the count signals cnt coming out of the PFD 220 and the window 1 signal en_pfd on output of the counter 218. For this example, N is set equal to 16. The next graph shows window 3, which is the combination gating signal of windows 1 and 2. The next four graphs show the up/down correction signals UP, DN for a locked condition on lines 208, 210 from the PFD 220 and the resulting up gate and down gate signals UPG, DNG at the output of gates 214 and 216, respectively.

[00030] By way of example, the window 1 or the frequency between cycles is in the range of 0.5 to 3.33 microseconds. This is a function of the frequency of the input signal 202. The width of window 2 (and, consequently, window 3) is in the range of 0.1 to 0.5 microseconds and preferably is under 0.5 microseconds. Thus, the correction cycle is limited. The time delay circuits 314, 324 may be changed to define the window 3 width. The PLL has been designed to have inertia such that it does not quickly change to overcompensate. This minimizes the effect of irregular

reference signals. This irregularity either being missing cycles or a varying in frequency.

[00031] Another embodiment to create the window 2 signal is illustrated in Figure 6. A second PFD 350 is provided as the second window circuit 300. The input signal 202 and the oscillator signal at 234 are provided to the PFD 350. PFD 350 has an internal time delay Δt, which is greater than any time delay in PFD 200. All circuits include inherent time delay. Thus, the time through PFD 350 is delayed relative to the path through PFD 200. Since a single second window pulse is required per cycle, the count pulse cnt 2 at PFD 350 is inputted into the AND gates 214, 216. As is well known, the count pulse in a PFD is the output of an AND gate for both an up and down corrections. Even when the PLL is in sync or locked, there are up and down signals. Thus, as an alternative, if a PFD does not include a count circuit, the up and down output out of the second PFD 350 could be combined in an AND gate and provided as a signal 332 to the AND gates 214, 216. It should be noted that the time delay within the PFD 350 may be provided by additional pairs of inverters. The same would hold true for the time delay circuits 314, 324 of Figure 4. Other well-known time delay circuits or elements may be used.

[00032] Although the up/down counter 218 has been described in the aforementioned applications as a decrementing counter 218 for the frequency divider, it can also be an incrementing counter for the frequency divider.

[00033] Another improvement to the PLL, as illustrated in Figures 7 and 8, is to change the transmission rate or frequency of the first window. This allows the system to respond differently during start-up and non-lock and during lock. Thus, it is basically changing the bandwidth of the response of the PLL. A rate selector circuit 400, as illustrated in Figure 7, monitors the charge on capacitor 230 of the filter 226. The amount of charge on capacitor 230 is a function of the operation of the charge pump circuit 220. The rate selector circuit 400 includes a switch or MOS FET 402, which senses the voltage at capacitor 230. Connected to the source of MOS FET 402 is a current source 404. Once the voltage of the capacitor 230 exceeds the threshold of the MOS FET 402, it sends an enabling signal through Schmitt trigger 406 to the counter 218. Prior to this point, counter 218 is disabled or has a count of one and, therefore, for each cycle, an enable pulse is transmitted through to the logic gates 214, 216. Thus, for every cycle, the up and down pulses

UP, DN on 208 and 210 are transmitted through as signals UPG and DNG. Thus, initially, the PLL will have a correction every comparison cycle. Once the system gets closer to lock, the voltage on the capacitor 230 is maintained high and, therefore, the counter 218 will slow down the correction frequency by the comparison cycle divided by N. By way of example, whereas the time for lock of a 300 kHz signal using the circuit of Figure 3 and N = 16 is 10 milliseconds, with a selector circuit 400, the lock time has been decreased to the range of 2.5 milliseconds.

[00034] Figure 8 shows another embodiment of the rate selector 400. In this case, the rate selector 410 has more than one adjustment value, wherein N may be 1 to M cycles. The rate selector 410 may be a state machine which senses various levels of voltage on the capacitor 230 and sets the appropriate rate to the counter 218. For example, using a count of 16, the various levels or thresholds may set a count of 2, 4, 8, 12, 16. Alternatively, the state machine, after reading a first threshold, may incrementally or sequentially increase the count of counter 218. Thus, the lock process may be initially sped up to get to lock faster and then slowed down to maintain lock. Thus, the PLLs of Figures 7 and 8 are variable bandwidth PLLs.

[00035] The combination of the two improvements of the PLL is illustrated in Figure 9. The second window circuit 300 of Figure 4 is combined with the rate selector 400 of Figure 7 or Figure 8. Thus, the PLL of Figure 9 not only has a variable bandwidth with speed-up of the initial phase of the loop, but it also includes a narrow transmission or correction window to accommodate for variations in the input or reference signal.

[00036] Figure 10 is a WAN transmitter/receiver 700 that can incorporate any of the PLLs of Figures 4, 5 and 6-9, according to an embodiment of the invention. In addition to the PFD 200, charge pump 220, VCO 206, frequency divider 218 (omitted from Figure 10 for clarity), window 2 circuit 300 and the filter 226 (omitted from Figure 10 for clarity), the PLL includes a terminal 718 for receiving the reference signal and a local-oscillator (LO) distributor 720 for distributing the output of the VCO 206 as an LO signal. In addition to the PLL, the transmitter/receiver 700 includes a transmitter 704 and a receiver 706. The transmitter 704 includes a mixer 722 that modulates the LO with a differential base-band data signal received from a computer (not shown) via data terminals

724, 762. The transmitter 704 then provides this modulated data signal to a transmit-terminal 728 for wireless transmission to a remote receiver (not shown). Similarly, the receiver 706 receives a modulated data signal from a remote wireless transmitter (not shown) via a terminal 730, and includes a mixer 732 that demodulates the received data signal with the LO signal and provides a differential demodulated data signal to the computer via the terminals 724 and 726. The PLL is operable to synchronize the LO signal from the VCO 206 to the reference signal received on terminal 718. The transmitter/receiver 700 also includes other circuits that are conventional and that are thus omitted from Figure 10 for brevity.

[00037] Figure 11 is a block diagram of a general-purpose computer system 820 that incorporates the graphics board 100 of Figure 1, according to an embodiment of the invention. The computer system 820 (e.g., personal or server) includes one or more processing units 821, system memory 822, and a system bus 823. The system bus 823 couples the various system components including the system memory 822 to the processing unit 821. The system bus 823 may be any of several types of busses (including a memory bus, a peripheral bus and a local bus) using any of a variety of bus architectures. The system memory 822 typically includes read-only memory (ROM) 824 and random-access memory (RAM) 825. Firmware 826 containing the basic routines that help to transfer information between elements within the computer system 820 is also contained within the system memory 822. The computer system 820 may further include a hard disk-drive system 827 that is also connected to the system bus 823. Additionally, optical drives (not shown), CD-ROM drives (not shown), floppy drives (not shown) may be connected to the system bus 823 through respective drive controllers (not shown) as well.

[00038] A user may enter commands and information into the computer system 820 through input devices such as a keyboard 840 and pointing device 842. These input devices, as well as others not shown, are typically connected to the system bus 823 through a serial port interface 846. Other interfaces (not shown) include Universal Serial Bus (USB) and parallel ports 840. A monitor 847 or other type of display device may also be connected to the system bus 823 via an interface such as the graphics card 100.

[00039] Although the present disclosure has been described and illustrated in detail, it is to be clearly understood that this is done by way of illustration and example

only and is not to be taken by way of limitation. The scope of the present disclosure is to be limited only by the terms of the appended claims.